

3 a plurality of data wirings formed on the substrate substantially orthogonal to  
4 the gate wirings;

5 a plurality of pixel electrodes formed in a plurality of pixel areas decided by  
6 the gate wirings and the data wirings and arranged in a matrix shape;

7 A thin film transistor formed in each of the pixel areas and structured planar  
8 type having an operating semiconductor layer formed on the substrate, a gate insulating film  
9 formed on the operating semiconductor layer, a gate electrode formed on the gate insulating  
10 film and connected to one of the gate wirings, first and second semiconductor layers formed  
11 on both sides of the operating semiconductor layer including impurity, a source electrode  
12 including the first semiconductor layer electrically connected to the pixel electrode via a  
13 contact window opened to first and second insulating layers laminated on the first  
14 semiconductor layer, and a drain electrode including the second semiconductor layer and  
15 connected to the data wirings; and

16 a plurality of storage capacitor electrodes using the first semiconductor layer  
17 as a first storage capacitor electrode, having a second storage capacitor electrode being  
18 formed between the first insulating film and the second insulating film and connected to a  
19 storage capacitor wiring maintained at a predetermined potential, wherein at least a first  
20 storage capacitor is structured by the first storage capacitor electrode, the first insulating film  
21 and the second storage capacitor electrode, and a second storage capacitor is structured by  
22 the second storage capacitor electrode, the second insulating film and the pixel electrode.